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10/730,713	11/26/2003	Chen-Kuo Sun	79777	4010

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EXAMINER	
WILLIAMS, DON J	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,713	SUN ET AL.	
	Examiner	Art Unit	
	Don Williams	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *1,3 and 5-12* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/26/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5, 7-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al in view of Metz (4,659,945).

As to claim 1, Sun et al discloses an optically clocked optoelectronic track and hold apparatus (20) comprising a diode bridge (30) comprising a first node, a second node, a third node, a fourth node, and a plurality of diodes (D1-D8) wherein plurality of diodes (D1-D8) comprises a first diode (D1) having a cathode operatively coupled to first node and an anode operatively coupled to second node, a second diode (D5) having a cathode operatively coupled to third node and an anode operatively coupled to the first node, a third diode (D3) having a cathode operatively coupled to fourth node and an anode operatively coupled to the second node, a fourth diode (D4) having a cathode operatively coupled to the third node and an anode operatively coupled to the fourth node; an input node operatively coupled to the first node of the diode bridge (30) capable of receiving an analog input signal (Vi); a first photodetector (S1-S4) having a cathode operatively coupled to the second node and an anode operatively coupled to a negative potential node (-V) and a second photodetector (S1-S4) having an anode

operatively coupled to the third node and a cathode operatively coupled to a positive potential (+V) and wherein first and second photodetectors (S1-S4) are capable of receiving an optical input clocking signal (from laser 21 via optical fibers 22-25), and capable of reverse biasing and forward biasing; a hold capacitor (Ch, 40) operatively coupled to the fourth node capable of tracking the analog input signal (Vi) when the diode bridge (30) is forward biased and capable of holding analog input signal (Vi) when diode bridge (30) switches from forward biased to reverse biased, (fig. 2, column 4, lines 6-30, column 5, lines 15-30). Sun et al also disclose that the bridge-type optoelectronic sample and hold circuit (20) easily combines the current source and switch in a single OE device, (column 9, lines 4-6). Sun et al fail to explicitly disclose a first current source operatively coupled to second node and a second current source operatively coupled to the third node of the diode bridge. Sun et al and Metz are related sample and hold circuits with a diode bridge capable of forward and reverse bias conditions. Metz discloses current sources (14, 16) transmitting currents (IS1, IS2), (fig. 4, column 3, lines 51-68, column 4, lines 1-8). It would have been obvious for one of ordinary skill in the art to modify Sun et al to include current sources as disclosed by Metz in order to generate high speed current signals to the diode bridge to allow forward biasing of the system allowing the system to perform at an optimal level.

As to claim 3, the modified Sun et al discloses two photodetectors (S1-S4) are reversed biased by voltage sources (+V, -V), (fig. 2, column 8, lines 15-20, lines 35-49).

As to claim 5, the modified Sun et al discloses a first optical input clocking signal (from laser 21 via optical fibers 22-25) and a second optical input clocking signal (from

laser 21 via optical fibers22-25) wherein first photodetector (S1-S4) is capable of receiving first optical input clocking signal (from laser 21 via optical fibers 22-25) and wherein second photodetector (S1-S4) is capable of receiving second optical input clocking signal (from laser 21 via optical fibers 22-25) and wherein first optical input clocking signal (from laser 21 via optical fibers 22-25) and second optical input clocking signal (from laser 21 via optical fibers 22-25) are synchronized, (fig. 2, column 4, lines 6-17, lines 44-55, column 5, lines 30-33).

As to claim 7, the modified Sun et al disclose first and second photodetectors (S3, S4) switches diode bridge (30) from reverse biased to forward biased when optical input clocking signal illuminates first and second photodetectors (S3, S4) with an optical pulse, (fig. 2, column 4, lines 6-18, column 5, lines 15-33).

As to claim 8, the modified Sun et al disclose first and second photodetectors (S3, S4) switches diode bridge (30) from reverse biased to forward biased when first and second photodetectors (S3, S4) do not generate enough photocurrent to reverse bias diode bridge (30), (fig. 2, column 5, lines 15-33).

As to claim 9, the modified Sun et al disclose optically clocked optoelectronic track and hold apparatus (20) is configured into a positive node device (+V) and a negative node device (-V) wherein optically clocked optoelectronic track and hold apparatus (20) receives analog input signal (Vi) and an inverted analog input signal and outputs a differential output signal (Vout), (fig. 2, column 4, lines 6-15, column 8, lines 15-49).

As to claim 10, the modified Sun et al disclose an amplifier (35) operatively coupled to hold capacitor (Ch, 40) capable of outputting a first track and hold output signal (Vout), (fig. 2, column 4, lines 26-32).

As to claim 12, the modified Sun et al disclose an electronic track and hold device (20) operatively coupled to amplifier (35) capable of receiving first track and hold output signal (Vout) and an electronic clock signal (from laser 21 via optical fibers 22-25), (fig. 2, column 4, lines 6-32). The modified Sun et al further disclose that Metz (fig. 7, column 7, lines 4-11) sets forth a sampling bridge with a first electronic track and hold device (12) being connected to a second electronic track and hold device (20) via output signal (Vo) wherein the electronic track and hold device (20) is capable of outputting a second track and hold output signal (Vout). It would have been obvious for one of ordinary skill in the art to further modify the modified Sun et al to include the second electronic track and hold device taught by Metz in order to provide a desired compensation to the output signal from the previous circuitry of the apparatus allowing high speed signal processing and transmission throughout the system.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al in view of Metz and further in view of MacDonald (4,727,349).

As to claim 6, the modified Sun et al further disclose that Metz (fig. 4, column 4, lines 17-28) sets forth clamped diodes (D1, D2) in a forward bias condition constitutes the rise and fall of sample voltage (Vi). The modified Sun et al in view of Metz fail to explicitly teach first and second photodetectors have fast rise times and long fall times.

MacDonald et al disclose a detector shows a fast rise time and long fall times, (column 1, lines 35-53). It would have been obvious for one of ordinary skill in the art to modify Sun et al in view of Metz by utilizing photodetectors having fast rise times and long fall times as taught by MacDonald et al in order to provide desired performance of the photodetectors allowing high speed signal switching for further processing and transmission of the device.

Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al in view of Metz and further in view of Taddiken (5,455,584).

As to claim 11, Sun et al in view of Metz fail to teach a quantizer capable of quantizing first track and hold output signal and outputting a digital output signal. Taddiken disclose high frequency high resolution quantizer having a quantizer (20) operatively coupled to an amplifier (16), capable of quantizing a track and hold output signal and outputting a digital output signal. It would have been obvious for one of ordinary skill in the art to further modify Sun et al in view of Metz to include a quantizer as taught by Taddiken in order to provide a desired formation of the output signal allowing high speed processing and signal transmission throughout the device.

Response to Arguments

Applicant's arguments filed May 29, 2007 have been fully considered but they are not persuasive. Claims 2 and 4 have been cancelled.

With respect to claim 1, the applicant states that the reference of Sun et al does not singly or in combination teach, disclose, or suggest an apparatus that comprise of a first through a fourth diode having respective cathodes and anodes connected to respective first through fourth nodes, an input node coupled to first node of a diode bridge, a first and second current source operatively coupled to respective nodes of the diode bridge, a first and second photodetector operatively coupled to respective nodes and capable of receiving an optical input clocking signal, and capable of reverse biasing and forward biasing the diode bridge in response to the optical input clocking signal, and a hold capacitor operatively coupled to respective node and capable of tracking and holding the analog input signal when the diode bridge switches from biased to reverse biased.

However, Sun et al (see fig. 2) explicitly disclose an optically clocked optoelectronic track and hold apparatus (20) comprising a diode bridge (30) having a first node, a second node, a third node, a fourth node, and a plurality of diodes (D1-D8) wherein plurality of diodes (D1-D8) comprises a first diode (D1) having a cathode operatively coupled to first node and an anode operatively coupled to second node, a second diode (D5) having a cathode operatively coupled to third node and an anode operatively coupled to the first node, a third diode (D3) having a cathode operatively coupled to fourth node and an anode operatively coupled to the second node, a fourth diode (D4) having a cathode operatively coupled to the third node and an anode operatively coupled to the fourth node; an input node operatively coupled to the first node of the diode bridge (30) capable of receiving an analog input signal (Vi); a first

photodetector (S1-S4) having a cathode operatively coupled to the second node and an anode operatively coupled to a negative potential node (-V) and a second photodetector (S1-S4) having an anode operatively coupled to the third node and a cathode operatively coupled to a positive potential (+V) and wherein first and second photodetectors (S1-S4) are capable of receiving an optical input clocking signal (from laser 21 via optical fibers 22-25), and capable of reverse biasing and forward biasing; a hold capacitor (Ch, 40) operatively coupled to the fourth node capable of tracking the analog input signal (Vi) when the diode bridge (30) is forward biased and capable of holding analog input signal (Vi) when diode bridge (30) switches from forward biased to reverse biased, (fig. 2, column 4, lines 6-30, column 5, lines 15-30). Sun et al also disclose that the bridge-type optoelectronic sample and hold circuit (20) easily combines the current source and switch in a single OE device, (column 9, lines 4-6). Sun et al and Metz are related sample and hold circuits with a diode bridge capable of forward and reverse bias conditions. Metz discloses current sources (14, 16) operatively coupled to respective nodes and transmitting currents (IS1, IS2), (fig. 4, column 3, lines 51-68, column 4, lines 1-8). Therefore because of the reasoning set forth above, the rejection is proper.

Allowable Subject Matter

Claims 15-20 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art fails to disclose either singly or in combination a method for optically clocked optoelectronic tracking and holding comprising the steps of maintaining a diode bridge in forward bias and returning to STEP(a) if an optical pulse is not received from an optical input clocking signal, switching the diode bridge to reverse bias for a desired time, and returning to STEP(a) if the optical pulse is received from the optical input clocking signal regarding claim (15) and an optically clocked optoelctronic track and hold apparatus comprising means for maintaining a diode bridge in forward bias if an optical pulse is not received from an optical input clocking signal; and means for switching the diode bridge to reverse bias for a desired time if an optical pulse is received from an input clocking signal regarding claim (20).

Claims 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose an optically clocked optoelectronic track and hold apparatus either singly or in combination having first and second photodetectors comprising a short transit time photodiode and a long transit time photodiode in a parallel configuration.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Williams whose telephone number is 571-272-8538. The examiner can normally be reached on 8:30a.m. to 5:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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